AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1. (original) A bit-rate detection circuit, comprising:

a plurality of shift registers adapted to serially shift in bits of data having a data frequency from a first transceiver, said shift registers being clocked at a first predetermined rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the data frequency.

2. (original) The bit-rate detection circuit of Claim 1 wherein said first predetermined rate is the highest possible data rate that the incoming data frequency can be.

3. (original) The bit-rate detection circuit of Claim 1 wherein said logic circuitry is coupled to nodes defined between said shift registers.

4. (original) The bit-rate detection circuit of Claim 3 wherein said logic circuitry comprises a first logic set and a second logic set each providing an output signal, said first logic set being coupled to a first set of said nodes between said shift registers, and said second logic set being coupled to a second set of said nodes between said shift registers.

5. (original) The bit-rate detection circuit of Claim 4 wherein said first logic set determines if said incoming data frequency is a first predetermined frequency, and said second logic set determines if said incoming data frequency is a second predetermined frequency being less than said first predetermined frequency.

6. (original) The bit-rate detection circuit of Claim 5 wherein said first predetermined frequency is a multiple of said second predetermined frequency.

7. (original) The bit-rate detection circuit of Claim 4 further comprising output logic circuitry responsively coupled to said first logic set and said second logic set, said output logic circuitry providing said output signal indicative of the data frequency.

8. (original) The bit-rate detection circuit of Claim 4 further comprising a third logic set coupled to a third set of said nodes being different than said first and second sets of nodes.

9. (original) The bit-rate detection circuit of Claim 8 wherein said third logic set determines if said incoming data frequency is a third predetermined frequency being less than said second predetermined frequency.

10. (original) The bit-rate detection circuit of Claim 9 wherein said first predetermined frequency is in multiple of said third predetermined frequency.

11. (original) The bit-rate detection circuit of Claim 10 wherein said third predetermined frequency is also a multiple of said second predetermined frequency.

12. (original) The bit-rate detection circuit of Claim 1 further comprising a communications transceiver module responsively coupled to said logic circuitry output signal and adapted to transmit data back to said first transceiver at said incoming data frequency.

13. (original) The bit-rate detection circuit of Claim 1 wherein said logic circuitry includes a single clock operating at a first frequency.

14. (original) The bit-rate detection circuit of Claim 1 wherein said logic circuit provides said output signal as a function of framing data clocked into said shift registers.

15. (original) The bit-rate detection circuit of Claim 14 wherein said framing data is A1 and A2 SONET framing bytes.

16. (original) A data transceiver, comprising:

a data receiver circuit;

logic circuitry responsively coupled to said receiver circuit determining a data rate of data received by said data receiver, said logic circuit including and operating off a single clock operating at a first predetermined frequency; and

a data transmitter responsively coupled to said logic circuitry and adapted to transmit data at a data rate as a function of said output signal.

17. (original) The bit-rate detection circuit of Claim 16 wherein said logic circuitry comprises;

a plurality of shift registers adapted to serially shift in data having a data frequency from a first transceiver, said shift registers being clocked at a first predetermined rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the incoming data frequency.

18. (original) The bit-rate detection circuit of Claim 17 wherein said first predetermined rate is the highest possible data rate that the incoming data frequency can be.

19. (original) The bit-rate detection circuit of Claim 17 wherein said logic circuitry is coupled to nodes defined between said shift registers.

20. (original) The bit-rate detection circuit of Claim 19 wherein said logic circuitry comprises a first logic set and a second logic set each providing an output signal, said first logic set being coupled to a first set of said nodes defined between said shift registers, and said second logic set being coupled to a second set of said nodes defined between said shift registers.

21. (original) A method of detecting a bit-rate of data incoming to a receiver, comprising the steps of:

a) clocking said incoming bit data at a first frequency into a plurality of shift registers having a node between each said shift register; and

b) analyzing data at a plurality of said nodes to determine the bit-rate of said incoming bit data.

22. (original) The method as specified in Claim 21 wherein said first frequency is the maximum possible data bit-rate of said incoming bit data.

23. (currently amended) The method as specified in Claim 22 wherein logic circuitry analyzes said bit data, said logic circuitry having a first logic set coupled to a first set of said nodes determining if said data bit-rate could be a first data rate, and a second logic set coupled to a second set of said nodes determining if said data bit-rate could be a second data rate being less than said first data rate.

24. (original) The method of Claim 23 wherein said first data rate is said first frequency, and said first data rate is also a multiple of said second data rate.

25. (original) The method of Claim 21 further comprising the step of responsively transmitting data from a transmitter at a data rate being said determined incoming data bit-rate.

26. (original) The method of Claim 21 wherein frame data is said analyzed data in said step b).

27. (original) The method of Claim 26 where in said frame data is a A1 and A2 SONET framing byte.

28. (original) A bit-rate detection circuit, comprising:

a plurality of shift registers adapted to shift in bits of data having a data rate in parallel from a first transceiver, said shift registers being clocked at a predetermined clock rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the data rate.

29. (original) The bit-rate detection circuit as specified in Claim 28, wherein said clock rate is less than the maximum data rate.

30. (original) The bit-rate detection circuit as specified in Claim 29, wherein said data rate is a multiple of said clock rate.